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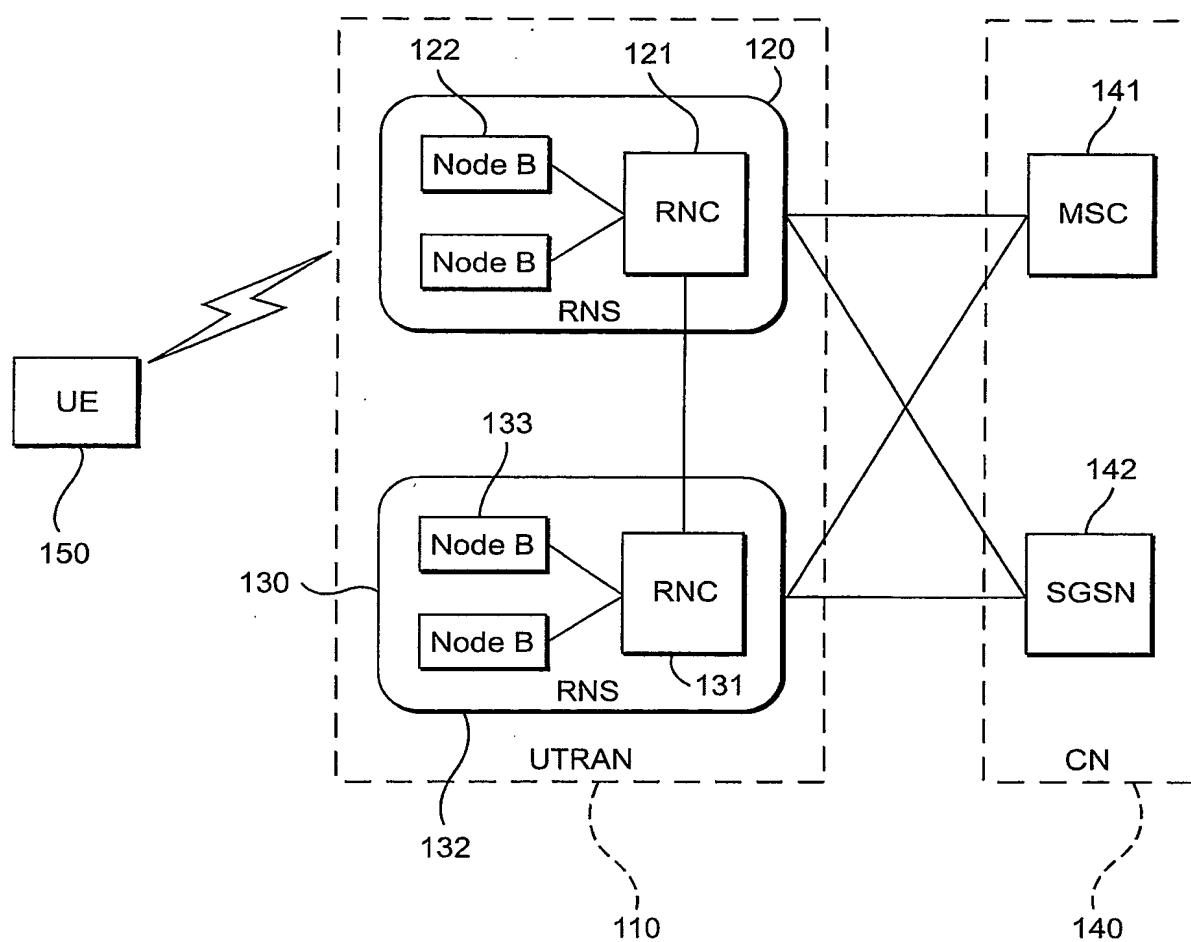


Fig. 1

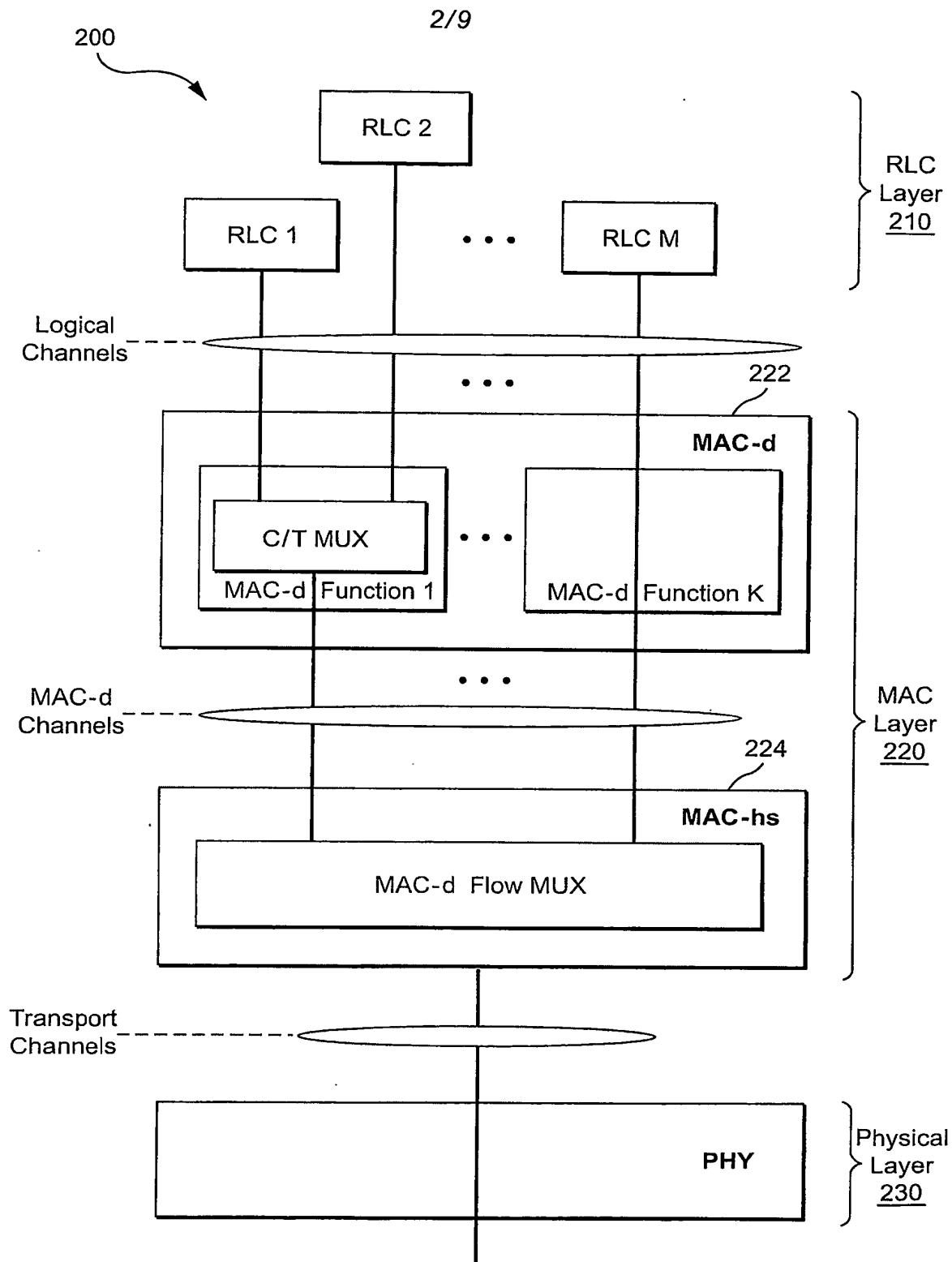


Fig. 2

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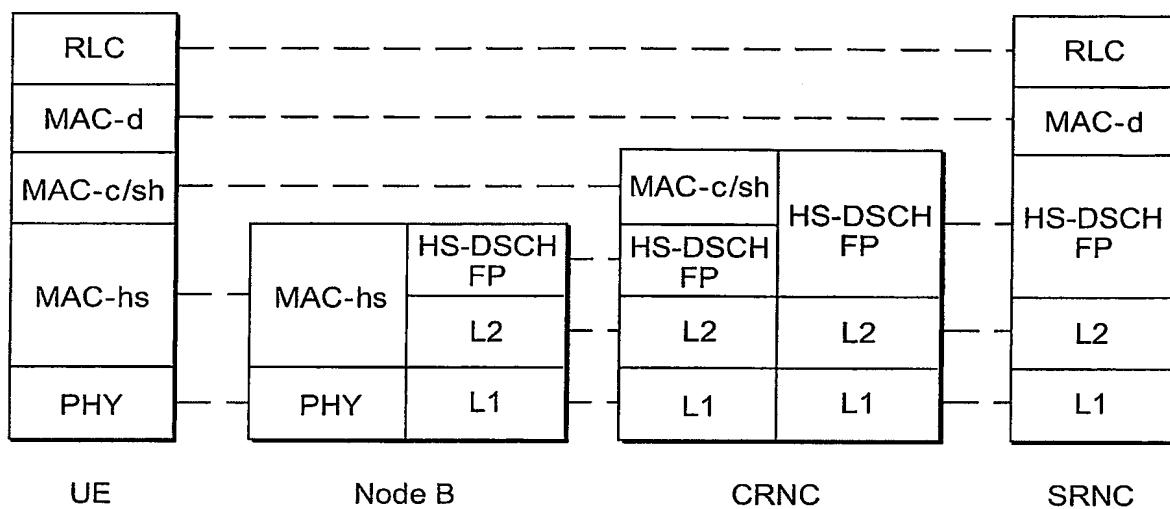


Fig. 3

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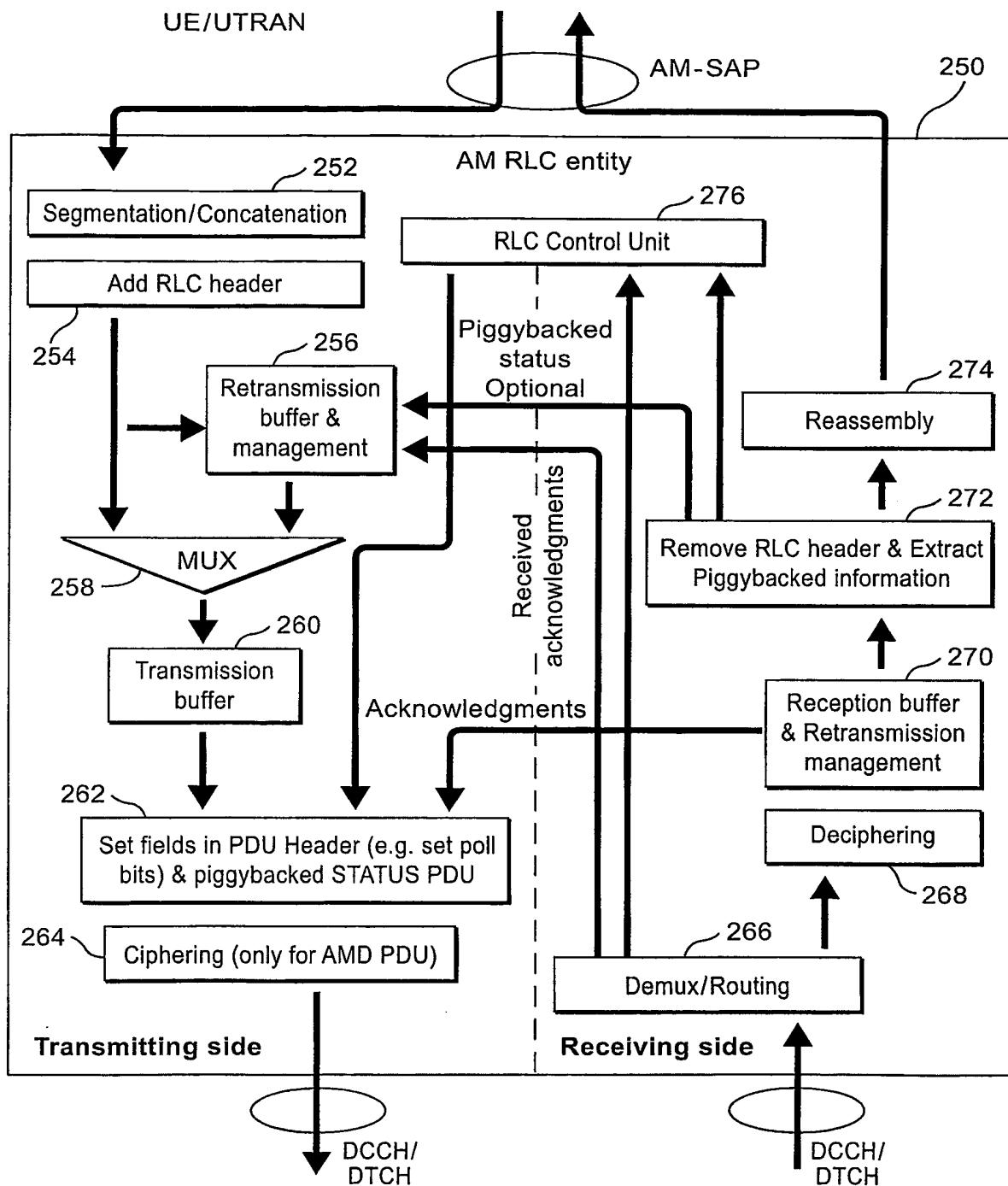


Fig. 4

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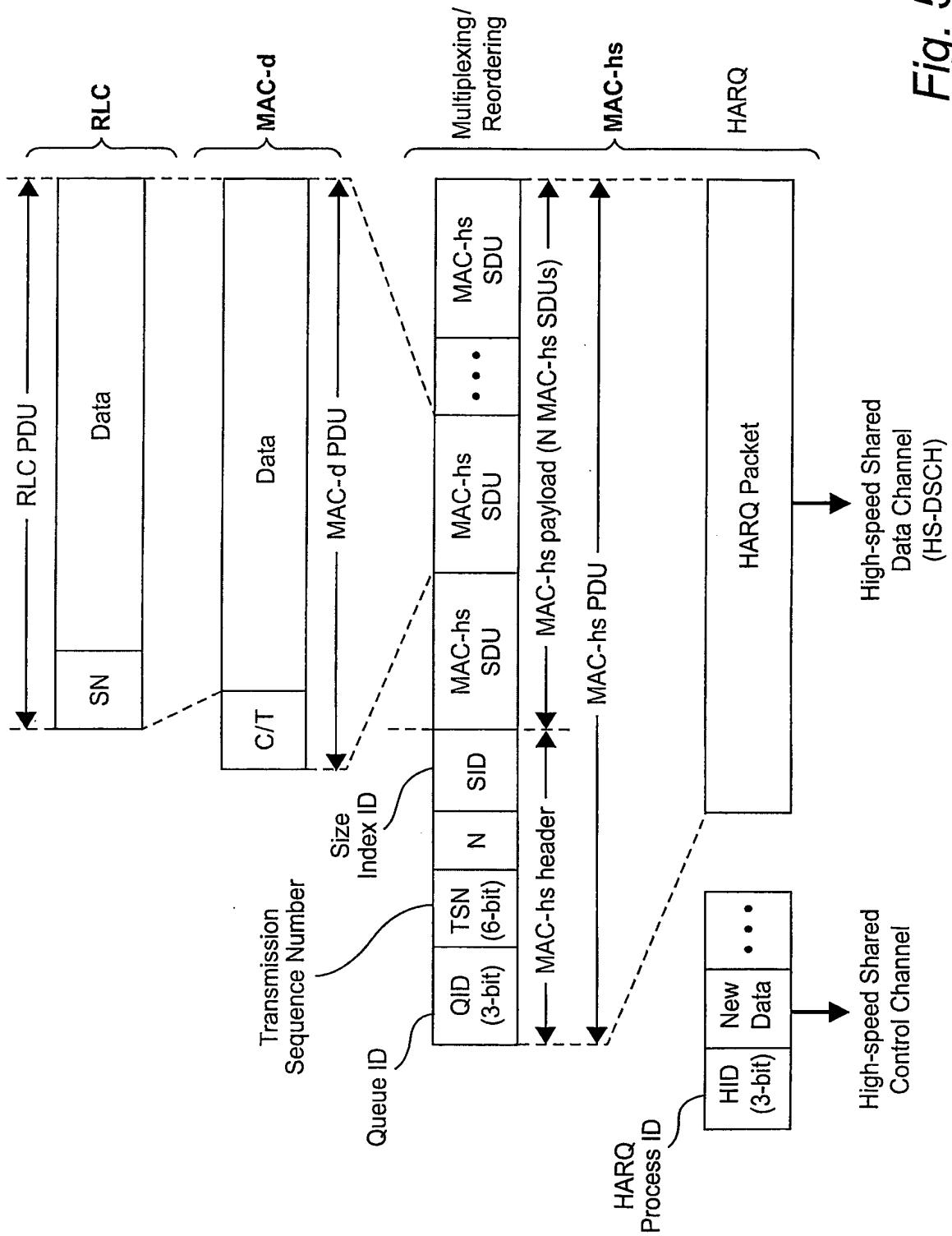
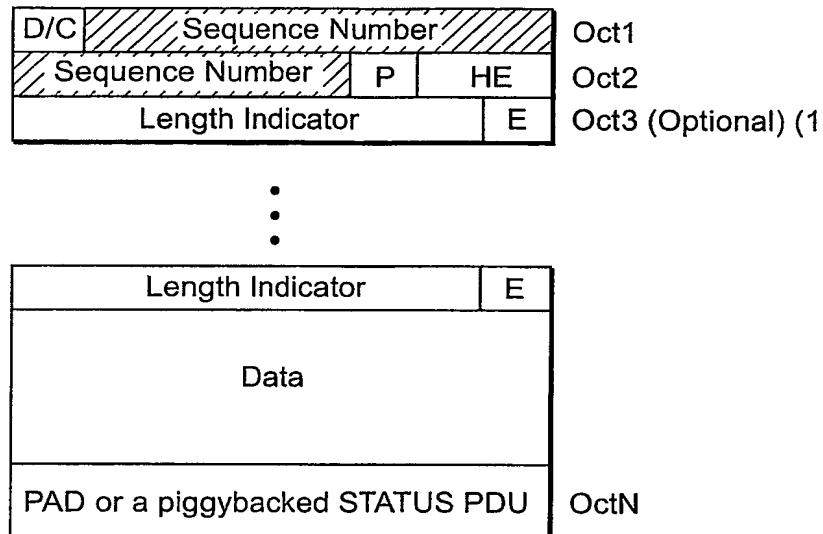
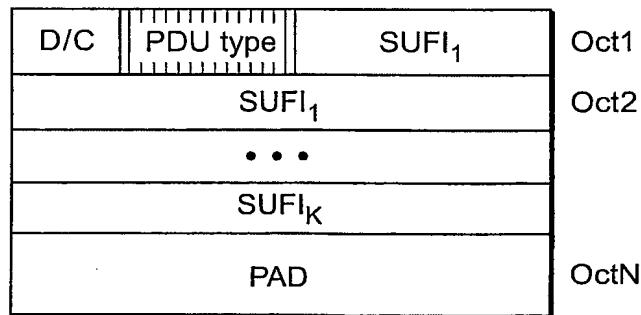


Fig. 5

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AM RLC PDU Header**AMD (Data) PDU***Fig. 6***Control PDU***Fig. 7*

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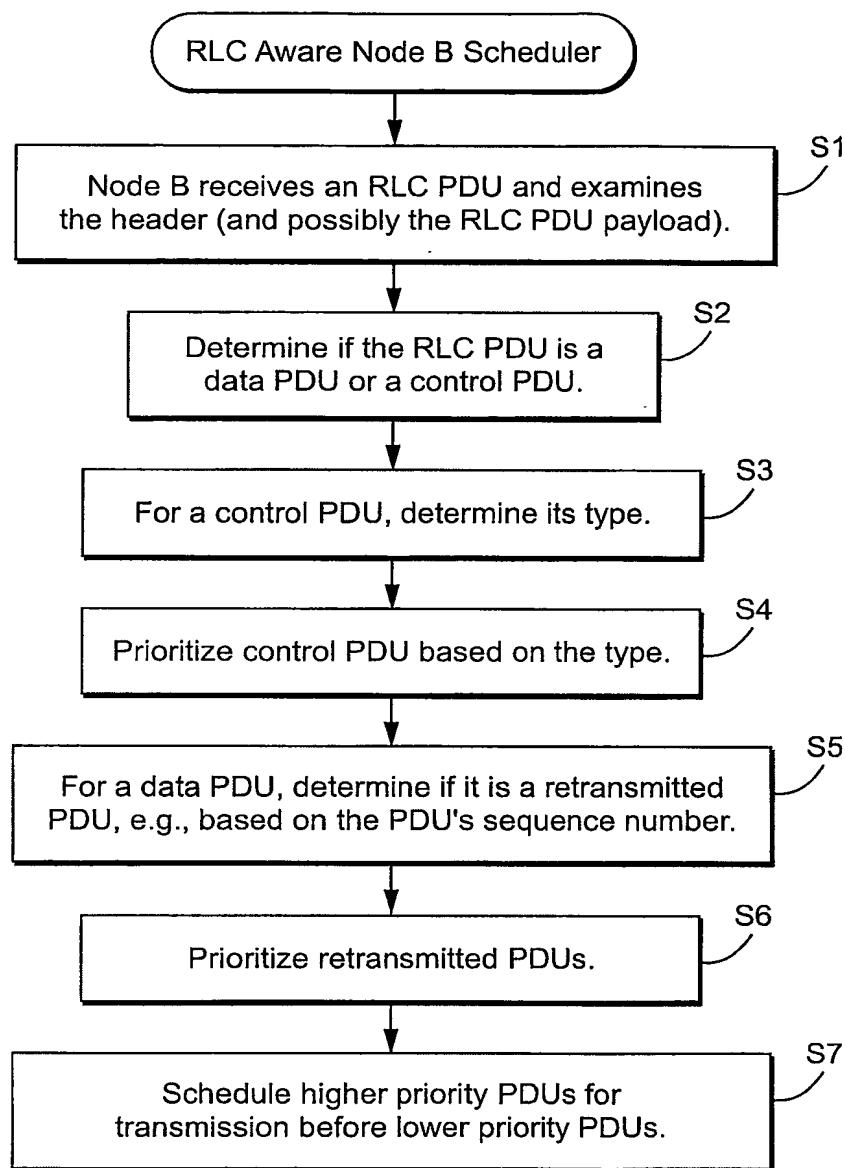
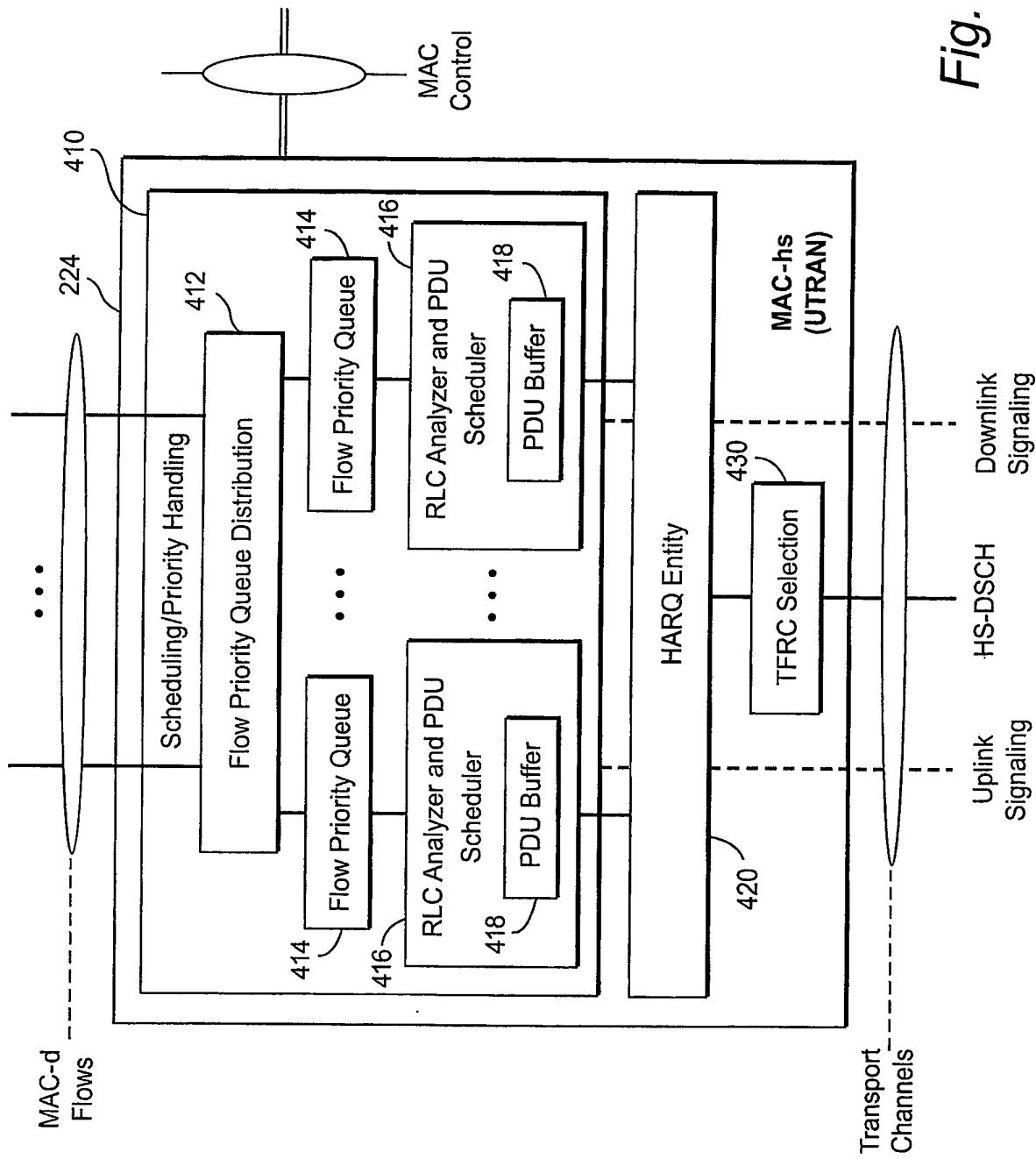


Fig. 8



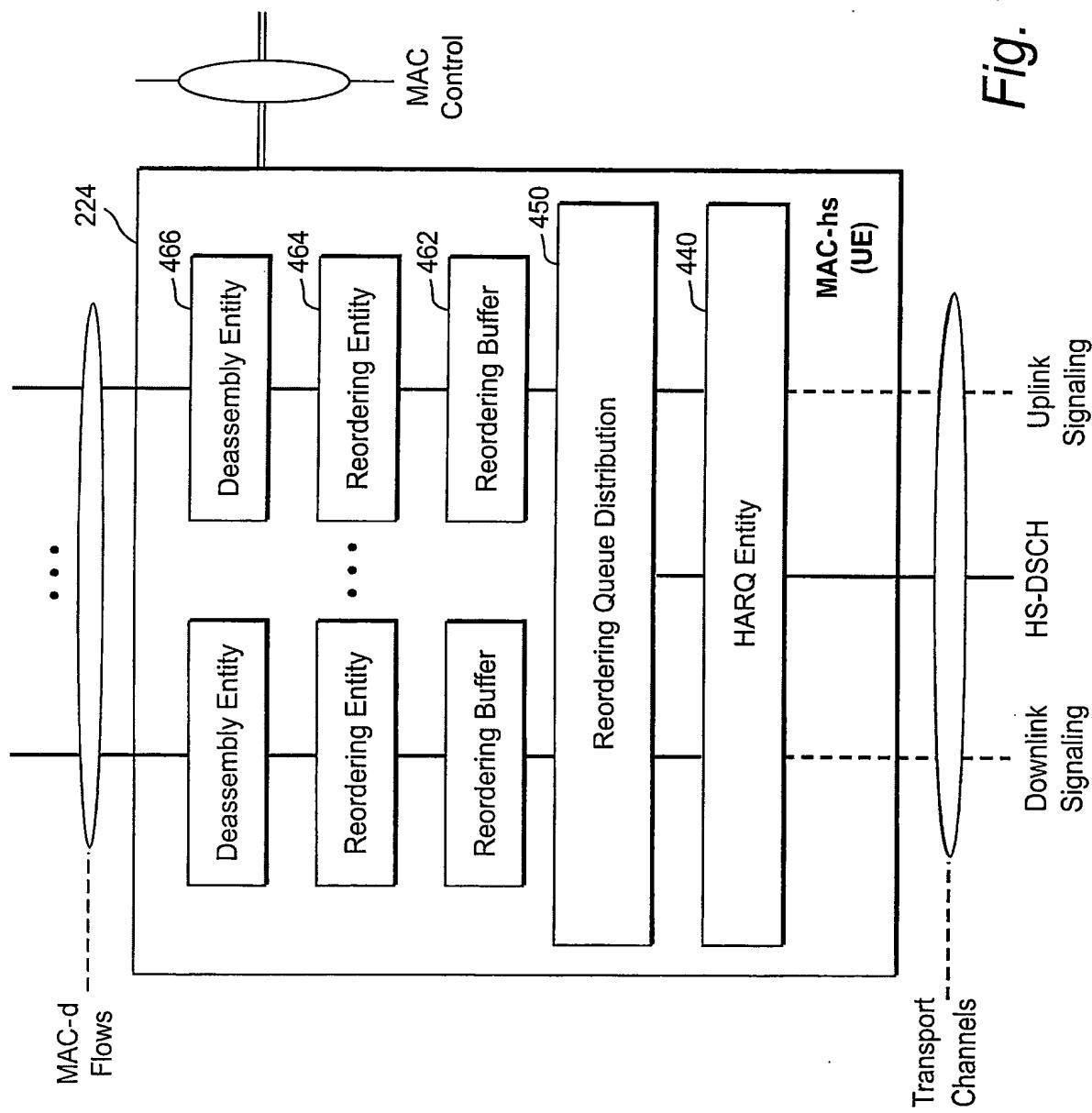


Fig. 10